Thomson Reuters Expert Witness Services
Consultant Curriculum Vitae

R. Jacob (Jake) Baker, Ph.D., P.E.

Expertise

- CMOS Circuit Design
- Analog Integrated Circuits
- Mixed-Signal Design
- Phase- and Delay-Locked Loops
- Power MOSFET Circuit Design
- Analog-to-Digital, Digital-to-Analog Conversion
- Delta-Sigma Techniques
- Power Electronics
- DRAM, Flash, Resistive Memory

Summary

- Active scholar (h-index of 27 and g-index of 62) whose research is focused on:
  - High-speed interfaces for electro-optic, mixed-signal, and analog integrated circuits;
  - Design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide);
  - Analog and mixed-signal circuit techniques for nanometer CMOS; 3D packaging techniques
  - Delivery of circuit design education to off-campus students/engineers via the Internet.
- Mentor to:
  - Approximately 75 graduate students (major professor), http://CMOSedu.com/jbaker/students/students.htm
  - Electrical and Computer Engineering Department faculty;
  - Engineers locally, nationally, and internationally;
  - New and established companies.
- Extensive leadership experience including:
  - Chair, Electrical and Computer Engineering Department, Boise State University;
  - Dealing with conflict, problems, and limited resources;
  - Leading the department through ABET accreditation;
  - Creation and implementation of both Master and Doctoral programs in ECE.
- Inventor with more than 200 granted or pending patents in integrated circuit design.

- Experienced integrated circuit designer and educator with significant industry experience. See additional information at http://cmosedu.com/jbaker/projects/fund.htm
- Textbook authorship and Internet contributions (see http://CMOSedu.com), that have helped tens of thousands of engineers around the world.
- Recognized by the IEEE Power Electronics Society with the Best Paper Award in 2000 (*IEEE Transactions on Power Electronics*) from PhD dissertation work.
- International known in the field of integrated circuit design, recipient of many honors including the Terman Award, the IEEE CAS Education Award, and IEEE Fellow.
- Outstanding educator, drawing significant interest in graduate and undergraduate integrated circuit design courses offered live and on the internet.

Employment History

From:	2012	**University of Nevada, Las Vegas**
To:	Present	Las Vegas, NV
	Position	*Professor of Electrical and Computer Engineering*

From:	2000	**Boise State University**
To:	2012	Boise, ID
	Position	*2003-2012: Professor of Electrical & Computer Engineering* *2004-2007: Department Chair* *2000-2003: Tenured Associate Professor*

From:	1993	**University of Idaho**
To:	2000	ID
	Position	*1998-2000: Tenured Associate Professor of Electrical Engineering* *1993-1998: Assistant Professor of Electrical Engineering* Assisted (on the department's ABET committee) with the preparation of the 2000 ABET accreditation report for the Electrical and Computer Engineering Department's fall 2000 visit

From:	1991	**University of Nevada**
To:	1993	Reno, NV and Las Vegas, NV
	Position	*Lecturer, Department of Electrical Engineering* Taught courses in circuits, communication systems, electronics, and material science.

Additional Details on University Employment

- Research focused on analog and mixed-signal integrated circuit design. Worked with multi-disciplinary teams (civil engineering, biology, materials science, etc.)

on projects that have been funded by EPA, DARPA, NASA and the Air Force Research Lab.

- Current research interests are:
  - Design of readout integrated circuits (ROICs) for use with focal plane arrays (FPAs)
  - Heterogeneous integration of III-V photonic devices (e.g. FPAs and VCSELs) with CMOS
  - Methods (e.g., 3D packaging and capacitive interconnects) to reduce power consumption in semiconductor memories
  - Analog and mixed-signal circuit design for communication systems, synchronization, and data conversion especially using the *K*-Delta-1-Sigma modulator
  - The design of writing and sensing circuitry for emerging nonvolatile memory technologies, focal planes, and displays (arrays) in nascent nanotechnologies (e.g. magnetic, chalcogenide)
  - Reconfigurable electronics design using nascent memory technologies
  - Finding an electronic, that is, no mechanical component, replacement for the hard disk drive using nascent fabrication technologies
  - Methods to deliver circuit design education to industry and off-campus students, see videos here
- Led, as chair, the department in graduate curriculum (MS and PhD), program development, and an ABET accreditation visits.
- Worked with established and start-up companies, to provide technical expertise and identify employment opportunities for students.
- Held various leadership and service positions including: ECE chair, graduate coordinator, college curriculum committee (chair), promotion and tenure committee, scholarly activities committee, faculty search committee, university level search committees, etc. Collaborate with College of Engineering faculty on joint research projects.
- Taught courses in circuits, analog IC design, digital VLSI, and mixed-signal integrated circuit design to both on- and, via the Internet, off-campus students. Research emphasis in integrated circuit design using nascent technologies.

From: 1994 **Micron Technology**
To: 2008

Position: *Affiliate Faculty (Senior Designer)*
Designed CMOS circuits for DRAMs including DLLs (design is currently used in Micron's DDR memory), PLLs for embedded graphics chips, voltage references and regulators, data converters, field-emitting display drivers, sensing for MRAM (using delta-sigma data conversion topologies), CMOS active pixel imagers and sensors, power supply design (linear and switching). Worked on a joint research project between Micron and HP labs in magnetic memory. Developed, designed, and tested circuit

design techniques for multi-level cell (MLC) Flash memory using signal processing. Considerable experience working with product engineering to ensure high-yield from the production line.

Co-authored a book on DRAM circuit design through the support of Micron. Gained knowledge in the entire memory design process from fabrication to packaging.

Developed, designed, and tested circuit design techniques for multi-level cell (MLC) Flash memory using signal processing (35 nm technology node).

From: 1985 **E.G.&G. Energy Measurements Inc.**
To: 1993 NV
Position: *Senior Electronics Design Engineer*
Responsible for the design and manufacturing of instrumentation used in support of Lawrence Livermore National Laboratory's Nuclear Test Program. Responsible for designing over 30 electronic and electro-optic instruments. This position provided considerable fundamental grounding in EE with a broad exposure to PC board design to the design of cable equalizers. Also gained experience in circuit design technologies including: bipolar, vacuum tubes (planar triodes for high voltages), hybrid integrated circuits, GaAs (high speed logic and HBTs), microwave techniques, fiber optic transmitters/receivers, etc.

Industrial Experience

2010 - present: Working with Arete' Associates on the design of high-speed compressive transimpedance amplifiers for LADAR projects and the design of ROIC unit cells. Work funded by the U. S. Air Force.

2010 - 2012: Working with Aerius Photonics (and then FLIR Inc. when Aerius was purchase by FLIR) on the design of Focal Plane Arrays funded (SBIRs and STTRs) by the U.S. Air Force, Navy, and Army. Experience with readout integrated circuits (ROICs) and the design/layout of photodectors in standard CMOS.

2009 - 2010: Contour Semiconductor, Inc. Design of NMOS voltage and current references as well as the design of a charge pump for an NMOS memory chip.

Summers 1994 - 1995: Micron Display Inc. Designing phase locked loop for generating a pixel clock for field emitting displays and a NTSC to RGB circuit on chip in NMOS. These displays are miniature color displays for camcorder and wrist watch size color television.

September - October 1993: Lawrence Berkeley Laboratory. Designed and constructed a 40 A, 2 kV power MOSFET pulse generator with a 3 ns risetime and 8 ns falltime for driving Helmholtz coils.

Summer 1993: Lawrence Livermore National Laboratory, Nova Laser Program. Researched picosecond instrumentation, including time-domain design for impulse radar and imaging.

Summer 1985: Reynolds Electrical Engineering Company, Las Vegas, Nevada. Gained hands on experience in primary and secondary power system design, installation and troubleshooting electric motors on mining equipment.

Consulting History

From: 2013 **Cirque, Inc.**
To: Present
Duties: Consulting on the design of analog-to-digital interfaces for capacitive touch displays and pads.

From: 2012 **Lockheed-Martin**
To:
Duties: CMOS circuit design for the development and manufacture of infrared components and imaging systems with an emphasis on highest sensitivity Indium Antimonide (InSb) focal plane arrays (FPAs) in linear through large staring formats. Product groups include FPAs, integrated dewar assemblies (IDCAs), camera heads, and infrared imaging systems.

From: 2009 **Sun Microsystems, Inc. (now Oracle)**
To: 2010 Austin, TX
Duties: VLSI research group. Provided consulting on memory circuit design and proximity connection (PxC) interfaces to DRAMs and SRAMs for lower power and 3D packaging.

From: 2008 **Nascentric**
To: Austin, TX
Duties: Provide directions on circuit operation (DRAM, memory, and mixed-signal) for fast SPICE circuit simulations.

From: 1997 **Tower Semiconductor**
To: 1998 Haifa, Israel
Duties: Designed CMOS integrated circuit cells for various modem chips.

From: 1998 **Amkor Wafer Fabrication Services, Micron Technology, and**

Rendition, Inc.

To:

Duties: Design PLLs and DLLs for custom ASICs and a graphics controller chip.

Litigation Support Experience

Date: 2013 **Morrison & Foerster LLP (Los Angeles, Palo Alto, and San Francisco, CA)**
Case STMicroelectronics, Inc. v. *InvenSense, Inc.*
Project: Provide expert consulting, non-infringement analysis, invalidity analysis, and wrote declaration.

Date: 2012-13 **Morgan, Lewis & Brockius LLP (Washington, DC)**
Case Elipda Memory, Inc. v. Nanya Technology Corporation, ITC Investigation No. 337-TA-819
Project: Provided expert consulting and reports on validity, infringement, and domestic industry. Provided declarations, deposition, and trial testimony.

Date: 2012 **Farella Braun + Martel LLP (San Francisco, CA)**
Case Round Rock Research LLC v. *Dell, Inc.*
Project: Provide expert consulting, non-infringement analysis, and invalidity analysis.

Date: 2012 **Morgan, Lewis & Brockius LLP (Palo Alto, CA)**
Case Nanya Technology Corporation v. Elipda Memory, Inc. and Kingston Technology Company, Inc., ITC Investigation No. 337-TA-821
Project: Provided expert consulting and reports on infringement, domestic industry, and validity. Provided Markman tutorial, declarations, deposition.

Date: 2012 **Farella Braun + Martel LLp (San Francisco, CA)**
Case Round Rock Research LLC v. Dell, Inc.
Project: Provide expert consulting, non-infringement analysis, and invalidity analysis.

Date: 2012 **Useful Arts IP (Cupertino, CA)**
Case Tezzaron (formerly Tachyon Semiconductor) v. Elm Technology
Project: Patent interference, wrote declaration, and provided deposition.

Date: 2011-12 **Wilson Sonsini Goodrich & Rosati PC (Palo Alto, CA)**
Case Panavision Imaging LLC v. *OmniVision Technologies, Inc.*
Project: Provide expert consulting, non-infringement analysis, invalidity analysis, two expert reports, and wrote declarations for summary judgment.

Date: 2011 **Latham & Watkins LLP (San Francisco, CA)**

Case Altera Corp. v. *LSI Corp. and Agere Systems, Inc.*
Project: Provide expert consulting, non-infringement analysis, and invalidity analysis.

Date: 2011 **Fish & Richardson PC (Washington, DC)**
Case Spansion LLC v. *Samsung Electronics Co., Ltd.*, Apple, Inc., Nokia Corp., PNY Technologies, Inc. Research In Motion Corporation, Transcend Information Inc., ITC Investigation No. 337-TA-735
Project: Provide expert consulting, non-infringement and invalidity analysis.

Date: 2010 **Jones Day LLP (Palo Alto, CA)**
Case LSI and Agere, Inc. v. *Xilinx, Inc.*
Project: Provide expert consulting, non-infringement analysis, and invalidity analysis.

Date: 2009 **Morrison & Foerster LLP (New York, NY)**
Case Innurvation, Inc. et al v. *Fujitsu Microelectronics America, Inc.*, Sony Corporation of America; Toshiba America Electronics Components, Inc.; Freescale Semiconductor, Inc.
Project: Provide expert consulting, non-infringement analysis, and invalidity analysis.

Date: 2009 **McDermott, Will, & Emery (Menlo Park, CA)**
Case Volterra Semiconductor Corp. v Primarion & Infineon Technologies North America & *Infineon Technologies, A.G*.
Project: Provide expert consulting, non-infringement analysis, invalidity analysis, deposition, and two expert reports.

1997-2008 Provided depositions and expert testimony in areas ranging from delay-locked loop design to fire alarm wiring reliability. Helped the Federal Trade Commission and International Trade Commission by providing explanations of how Rambus technology works and how it relates to mainstream DRAM interfaces for synchronous DRAMS.

Education

Year	College/University	Degree
1993	University of Nevada, Reno	Ph.D., Electrical Engineering
1988	University of Nevada, Las Vegas	MS, Electrical Engineering

Year	College/University	Degree
1986	University of Nevada, Las Vegas	BS, Electrical Engineering

Patents

Patent Number	Date Issued	Title
8,395,947	03/12/2013	Increased DRAM-array throughput using inactive bitlines
8,289,772	10/16/2012	Memory with correlated resistance
8,218,708	07/10/2012	Phase splitter using digital delay locked loops
8,194,477	06/05/2012	Subtraction circuits and digital-to-analog converters for semiconductor devices
8,149,646	04/03/2012	Digital Filters for Semiconductor Devices
8,117,520	02/14/2012	Error detection for multi-bit memory
8,102,295	01/24/2012	Integrators for delta-sigma modulators
8,098,180	01/17/2012	Devices including analog-to-digital converters for internal storage locations
8,093,643	01/10/2012	Multi-resistive integrated circuit memory
8,089,387	01/03/2012	Quantizing circuits with variable parameters
8,068,367	11/29/2011	Reference current sources
8,068,046	11/29/2011	Methods of quantizing signals using variable reference signals
8,042,012	10/18/2011	Systems and devices including memory with built-in self test and methods of making using the same
7,969,783	06/28/2011	Memory with correlated resistance
7,941,056	05/10/2011	Optical interconnect in high-speed memory systems
7,916,054	03/29/2011	K-delta-1-sigma modulator
7,877,623	01/25/2011	Method and apparatus for providing symmetrical output data for a double data rate DRAM
7,873,131	01/18/2011	Phase splitter using digital delay locked loops
7,869,249	01/11/2011	Complementary bit PCRAM sense amplifier and method of operation
7,839,703	11/23/2010	Subtraction circuits and digital-to-analog converters for semiconductor devices
7,830,729	11/09/2010	Digital filters with memory
7,818,638	10/19/2010	Systems and devices including memory with built-in self test and methods of making using the same
7,817,073	10/19/2010	Integrators for delta-sigma modulators
7,768,868	08/03/2010	Digital filters for semiconductor devices
7,733,262	06/08/2010	Quantizing circuits with variable reference signals
7,667,632	02/23/2010	Quantizing circuits for semiconductor devices
7,642,591	01/05/2010	Multi-resistive integrated circuit memory
7,616,474	11/10/2009	Offset compensated sensing for a magnetic random access memory
7,577,044	08/18/2009	Resistive memory element sensing using averaging

Patent Number	Date Issued	Title
7,538,702	05/26/2009	Quantizing circuits with variable parameters
7,528,877	05/05/2009	Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors
7,515,188	04/07/2009	Method and system for reducing mismatch between reference and intensity paths in analog to digital converters in CMOS active pixel sensors
7,495,964	02/24/2009	Method and apparatus for sensing flash memory using delta-sigma modulation
7,489,575	02/10/2009	Noise resistant small signal sensing circuit for a memory device
7,456,885	11/25/2008	Per column one-bit ADC for image sensors
7,449,953	11/11/2008	Input buffer design using common-mode feedback
7,421,607	09/02/2008	Method and apparatus for providing symmetrical output data for a double data rate DRAM
7,372,717	05/13/2008	Methods for resistive memory element sensing using averaging
7,366,021	04/29/2008	Method and apparatus for sensing flash memory using delta-sigma modulation
7,366,003	04/29/2008	Method of operating a complementary bit resistance memory sensor and method of operation
7,330,390	02/12/2008	Noise resistant small signal sensing circuit for a memory device
7,319,620	01/15/2008	Input and output buffers having symmetrical operating characteristics and immunity from voltage variations
7,310,018	12/18/2007	Method and apparatus providing input buffer design using common-mode feedback
7,286,428	10/23/2007	Offset compensated sensing for a magnetic random access memory
7,271,635	09/18/2007	Method and apparatus for reducing duty cycle distortion of an output signal
7,268,603	09/11/2007	Method and apparatus for reducing duty cycle distortion of an output signal
7,251,177	07/31/2007	Skewed sense AMP for variable resistance memory sensing
7,242,603	07/10/2007	Method of operating a complementary bit resistance memory sensor
7,237,136	06/26/2007	Method and apparatus for providing symmetrical output data for a double data rate DRAM
7,224,632	05/29/2007	Rewrite prevention in a variable resistance memory
7,151,689	12/19/2006	Integrated charge sensing scheme for resistive memories
7,133,307	11/07/2006	Adjusting the frequency of an oscillator for use in a resistive sense amp
7,123,525	10/17/2006	Phase detector for all-digital phase locked and delay locked loops
7,109,545	09/19/2006	Integrated circuit memory with offset capacitor
7,102,932	09/05/2006	Input and output buffers having symmetrical operating characteristics and immunity from voltage variations
7,095,667	08/22/2006	Noise resistant small signal sensing circuit for a memory device

Patent Number	Date Issued	Title
7,082,045	07/25/2006	Offset compensated sensing for a magnetic random access memory
7,009,901	03/07/2006	System and method for sensing data stored in a resistive memory element using one bit of a digital count
7,002,833	02/21/2006	Complementary bit resistance memory sensor and method of operation
6,987,701	01/17/2006	Phase detector for all-digital phase locked and delay locked loops
6,985,375	01/10/2006	Adjusting the frequency of an oscillator for use in a resistive sense amp
6,954,392	10/11/2005	Method for reducing power consumption when sensing a resistive memory
6,954,391	10/11/2005	Noise resistant small signal sensing circuit for a memory device
6,954,390	10/11/2005	Noise resistant small signal sensing circuit for a memory device
6,950,487	09/27/2005	Phase splitter using digital delay locked loops
6,930,942	08/16/2005	Method and apparatus for measuring current as in sensing a memory cell
6,917,534	07/12/2005	Offset compensated sensing for a magnetic random access memory
6,914,838	07/05/2005	Dual loop sensing scheme for resistive memory elements
6,914,454	07/05/2005	High speed low power input buffer
6,913,966	07/05/2005	Method for stabilizing or offsetting voltage in an integrated circuit
6,909,656	06/21/2005	PCRAM rewrite prevention
6,901,020	05/31/2005	“Integrated charge sensing scheme for resistive memories
6,888,771	05/03/2005	Skewed sense AMP for variable resistance memory sensing
6,885,580	04/26/2005	Method for reducing power consumption when sensing a resistive memory
6,882,578	04/19/2005	PCRAM rewrite prevention
6,870,784	03/22/2005	Integrated charge sensing scheme for resistive memories
6,859,383	02/22/2005	Sensing method and apparatus for a resistive memory device
6,856,564	02/15/2005	Noise resistant small signal sensing circuit for a memory device
6,856,532	02/15/2005	Offset compensated sensing for a magnetic random access memory
6,829,188	12/07/2004	Dual loop sensing scheme for resistive memory elements
6,826,102	11/30/2004	Noise resistant small signal sensing circuit for a memory device
6,822,892	11/23/2004	Resistive memory element sensing using averaging
6,813,208	11/02/2004	System and method for sensing data stored in a resistive memory element using one bit of a digital count
6,809,981	10/26/2004	Wordline driven method for sensing data in a resistive memory array
6,798,705	09/28/2004	Noise resistant small signal sensing circuit for a memory device
6,795,359	09/21/2004	Methods and apparatus for measuring current as in sensing a memory cell
6,791,859	09/14/2004	Complementary bit PCRAM sense amplifier and method of operation

Patent Number	Date Issued	Title
6,785,156	08/31/2004	Method and apparatus for sensing resistance values of memory cells
6,779,126	08/17/2004	Phase detector for all-digital phase locked and delay locked loops
6,774,690	08/10/2004	Digital dual-loop DLL design using coarse and fine loops
6,771,249	08/03/2004	Producing walking one pattern in shift register
6,741,490	05/25/2004	Sensing method and apparatus for resistance memory device
6,704,881	03/09/2004	Method and apparatus for providing symmetrical output data for a double data rate DRAM
6,687,179	02/03/2004	Method and system for writing data in an MRAM memory device
6,683,475	01/27/2004	High speed digital signal buffer and method
6,600,343	07/29/2003	High speed low power input buffer
6,597,600	07/22/2003	Offset compensated sensing for magnetic random access memory
6,577,525	06/10/2003	Sensing method and apparatus for resistive memory device
6,567,297	05/20/2003	Method and apparatus for sensing resistance values of memory cells
6,538,473	03/25/2003	High-speed digital signal buffer and method
6,509,245	01/21/2003	Electronic device with interleaved portions for use in integrated circuits
6,504,750	01/7/2003	Resistive memory element sensing using averaging
6,483,347	11/19/2002	High-speed digital signal buffer and method
6,445,231	09/03/2002	Digital dual-loop DLL design using coarse and fine loops
6,424,684	07/23/2002	Method and apparatus for receiving synchronous data
6,410,955	06/25/2002	Comb-shaped capacitor for use in integrated circuits
6,407,588	06/18/2002	High-speed, low-power input buffer
6,316,976	11/13/2001	Method and apparatus for improving the performance of digital delay locked loop circuits
6,256,234	07/03/2001	Low skew differential receiver with disable feature
6,104,209	08/15/2000	Low skew differential receiver with disable feature
6,069,506	05/30/2000	Method and apparatus for improving the performance of digital delay locked loop circuits
6,026,051	02/15/2000	Low skew differential receiver with disable feature
6,026,050	02/15/2000	Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same (continuation)
5,953,284	09/14/1999	Method and apparatus for adaptively adjusting the timing of a clock signal used to latch digital signals, and memory device using same
5,953,276	09/14/1999	Fully-differential amplifier
5,909,201	06/1/1999	Timing Control for a Matrixed Scanned Array
5,894,293	04/13/1999	Field emission display having pulsed capacitance current control
5,874,830	02/23/1999	Adaptively biased voltage regulator and operating method
5,818,365	10/01/1998	Serial to Parallel Conversion with a Phase-Locked Loop
5,638,085	06/10/1997	Timing Control for a Matrixed Scanned Array
5,614,856	03/25/1997	Waveshaping circuit generating two rising slopes for a sense amplifier pulldown device

Patent Number	Date Issued	Title
5,598,156	01/28/1997	Serial to Parallel Conversion with a PLL

Publications

Textbooks Authored:

1. Baker, R. J., "CMOS Circuit Design, Layout and Simulation, Third Edition," *Wiley-IEEE*, 1174 pages. ISBN 978-0470881323 (2010) Over 40,000 copies of this book's three editions in print.
2. Baker, R. J., "CMOS Mixed-Signal Circuit Design," *Wiley-IEEE*, 329 pages. ISBN 978-0470290262 (second edition, 2009) and ISBN 978-0471227540 (first edition, 2002)
3. Keeth, B., R.J. Baker, B. Johnson, and F. Lin "DRAM Circuit Design: Fundamental and High-Speed Topics," *Wiley-IEEE*, 2008, 201 pages. ISBN: 978-0-470-18475-2
4. Keeth, B. and R.J. Baker, "DRAM Circuit Design: A Tutorial," *Wiley-IEEE*, 2001, 201 pages. ISBN 0-7803-6014-1
5. Baker, R.J., Li, H.W., and Boyce, D.E. "CMOS Circuit Design, Layout and Simulation," *Wiley-IEEE*, 1998, 904 pages. ISBN 978-0780334168

Books, other (edited, chapters, etc.):

1. Saxena, V. and Baker, R.J. "Analog and Digital VLSI," chapter in the CRC Handbook on Industrial Electronics, edited by J.D. Irwin and B.D. Wilamowski, *CRC Press*, 2009 second edition.
2. Li, H.W., Baker, R.J., and Thelen D., "CMOS Amplifier Design," chapter 19 in the CRC VLSI Handbook, edited by Wai-kai Chen, *CRC Press*, 1999 (ISBN 0-8493-8593-8) and the second edition in 2007 (ISBN 978-0-8493-4199-1)
3. Baker, R.J. "CMOS Analog Circuit Design," (A self-study course with study guide, videos, and tests.) IEEE Education Activity Department, 1999. ISBN 0-7803-4822-2 (with textbook) and ISBN 0-7803-4823-0 (without textbook)
4. Baker, R.J., "CMOS Digital Circuit Design," (A self-study course with study guide, videos, and tests.) *IEEE Education Activity Department*, 1999. ISBN 0-7803-4812-5 (with textbook) and ISBN 0-7803-4813-3 (without textbook)

Refereed Journal Papers:

1. Harvard, Q. I. and Baker, R. J. "Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design," *in preparation*.

2. Estrada, D., Ogas, M.L., Southwick III, R.G., Price, P.M., Baker, R. J., Knowlton, W.B., *Impact of Single pMOSFET Dielectric Degradation on NAND Circuit Performance* (2008), Microelectronics Reliability, Vol. 48, No. 3, pp 354-363.
3. Leslie, M.B., and Baker, R.J., (2006) "Noise-Shaping Sense Amplifier for MRAM Cross-Point Arrays," *IEEE Journal of Solid State Circuits*, Vol. 41, No. 3, pp. 699-704.
4. Hess, H.L., and R.J. Baker., (2000) "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOS Devices," *IEEE Transactions on Power Electronics*, Vol. 15, No. 5, pp. 923-930.
5. Lin, F., Miller J., Schoenfeld A., Ma, M. and Baker, R.J., (1999) "A Register-Controlled Symmetrical DLL for Double-Data-Rate DRAM," *IEEE Journal of Solid State Circuits*, Vol. 34, No. 4, pp. 565-568.
6. Bruce, J.D., Li H.W., Dallabetta, M.J. and Baker, R.J., (1996) "Analog layout using ALAS!" *IEEE Journal of Solid State Circuits*, Vol. 31, No. 2, pp. 271-274.
7. Li H.W., Dallabetta M.J., and Baker R.J. (1995) "An interactive impulse response extraction system," *Review of Scientific Instruments* 66(10), 5092-5095.
8. Ward, S.T., Baker, R.J. and Li. H.W., (1995) "A microchannel plate image intensifier gating circuit capable of pulse widths from 30 ns to 10 us," *Measurement Science and Technology*, Vol. 6, No. 11, pp. 1631-1633.
9. Keeth, B., R. J. Baker, and H. W. Li., (1995) "CMOS transconductor VCO with adjustable operating and center frequencies," *Electronics Letters* 31(17), 1397-98.
10. Baker, R. J., (1994) "Time domain operation of the TRAPATT diode for picosecond-kilovolt pulse generation," *Review of Scientific Instruments* 65(10), 3286-88.
11. Baker, R. J. and S. T. Ward, (1994) "Designing nanosecond high voltage pulse generators using power MOSFETs," *Electronics Letters* 30(20), 1634-35.
12. Baker, R. J. and B. P. Johnson, (1994) "Sweep circuit design for a picosecond streak camera," *Measurement Science and Technology* 5(4).
13. Baker R. J., D. J. Hodder, B. P. Johnson, P. C. Subedi, and D. C. Williams, (1993) "Generation of kilovolt-subnanosecond pulses using a nonlinear transmission line" *Measurement Science and Technology* 4(8), 893-95.
14. Baker R. J. and Johnson B. P., (1993) "Series operation of power MOSFETs for high speed, high voltage switching applications," *Review of Scientific Instruments* 65(6).
15. Baker R. J. and Johnson B. P., (1993) "Applying the Marx bank circuit configuration to power MOSFETs," *Electronics Letters* 29(1), 56-57.
16. Baker R. J. and Johnson B. P., (1992) "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments* 63(12), 5799-5801.

17. Baker R. J. and Johnson B. P., (1992) "A 500 Volt nanosecond pulse generator using cascode connected power MOSFETs," *Measurement Science and Technology* 3 (8), 775-77.
18. Baker R. J., Perryman G. T., and Watts P. W., (1991) "A fiber-optically triggered avalanche transistor," *IEEE Transactions on Instrumentation and Measurement* 40(3), 649-52.
19. Baker R.J. (1991) "High voltage pulse generation using current mode second breakdown in a bipolar junction transistor," *Review of Scientific Instruments* 62(4), 1031-1036.
20. Baker R.J. and Pocha, M.D. (1990) "Nanosecond switching using power MOSFETs," *Review of Scientific Instruments* 61(8), 2211-2213.

Invited Talks and Seminars

Over 50 invited talks at conferences and Universities including: AMD, Arizona State University, Carnegie Mellon University, Dublin City University, Hong Kong University of Science and Technology, Indian Institute of Science (Bangalore, India), Iowa State University, Temple University, University of Alabama, University of Arkansas, University of Illinois, Urbana-Champaign, Utah State University, University of Nevada, Las Vegas, University of Houston, University of Idaho, University of Nevada, Reno, University of Macau, University of Utah, Yonsei University, University of Maryland, IEEE Electron Devices Conference (NVMTS), the Franklin Institute, National Semiconductor, AMI semiconductor, Micron Technology, Rendition, Sun Microsystems, Stanford University, ST Microelectronics (Delhi, India), Tower (Israel), Foveon, ICySSS keynote, Xilinx, etc.

Selected Talks

1. Baker, R. J., and Saxena, V., (2009-2010) "A K-Delta 1-Sigma Modulator for Wideband Analog-to-Digital Conversion," presented at various universities and companies.
2. Li, K., Saxena, V., and Baker, R. J., (2008) "The Baker ADC: An Overview," an online seminar in Windows Media format found here.

3. Saxena, V., and Baker, R. J., (2007-2008) "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs," presented at various universities and companies. Vishal Saxena Opamps Matlab Design Kit.zip
4. Baker, R. J., (2006-2008) "Circuit Design for MLC Flash: Towards a Semiconductor Replacement for the Hard Disk Drive," presented at various universities and companies.
5. Baker, R. J., (2007) Terman Award Acceptance Speech, given at the Frontiers in Education Conference (FIE 2007), Milwaukee, WI, October 11, 2007.
6. Baker, R. J., (2007) "The One-Transistor, One-Capacitor (1T1C) Dynamic Random Access Memory (DRAM), and its Impact on Society," presented at the Franklin Institute, in the symposium honoring Dr. Robert H. Dennard and his receipt of the 2007 Benjamin Franklin Medal in Electrical Engineering, April 25, 2007.
7. Baker, R. J. and Saxena, V., (2007) "Design of Bandpass Delta Sigma Modulators: Avoiding Common Mistakes," presented at various universities and companies.
8. Baker, R. J., (2001-2006) "Sensing Circuits for Resistive Memory," presented at various universities and companies.
9. Hadrick, M. and Baker, R. J., (2005) "Sensing in CMOS Imagers using Delta-Sigma Modulation," a general presentation of our work in this area.
10. Baker, R. J., (2005) "Design of High-Speed CMOS Op-Amps for Signal Processing," *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2005
11. Baker, R. J., (2004) "Delta-Sigma Modulation for Sensing," *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2004
12. Rivera, B. and Baker, R. J., (2001) "Design and Layout of Schottky Diodes in a Standard CMOS Process," *MURI Review*, November, 2001.

Research Funding

Recent funding listed below. In-kind, equipment, and other non-contract/grant funding [e.g., MOSIS support, money for travel for invited talks, etc.] not listed.

1. Campbell, K. A. and Baker, R. J., (2009-2012) "Reconfigurable Electronics and Non-Volatile Memory Research" funded by the Air Force Research Laboratory, $2,790,081
2. Baker, R. J., (2010-2012) "Dual Well Focal Plane Array (FPA) Sensor," U.S. Navy, $31,500
3. Baker, R. J., (2011) "Readout-Integrated Circuit (ROIC) Development in Support of Corrugated Quantum Well Infrared Photo-detector (C-QWIP) Focal Plane Arrays (FPA) for Tactical Applications," U.S. Army, $27,000

4. Baker, R. J., (2011) "Monolithic CMOS LADAR Focal Plane Array (FPA) with a Photonic High-Speed Output Interface," U.S. Air Force/DOD, $50,002
5. Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2008-2010) "Radiation Resistant Phase Change Memory and Reconfigurable Electronics," NASA. $1,500,000
6. Campbell, K. A., Baker, R. J., Peloquin, J., and Teasdale, J. (2007) "Reliability Investigations of Radiation Resistant, Multi-State Phase-Change Memory," NASA. $726,768
7. Baker, R. J., et. al., (2006-2010) "Establishment of a Doctoral Degree Program in Electrical and Computer Engineering in Electrical and Computer Engineering," Micron Foundation. $5,000,000
8. Baker, R. J., (2005-2006) "Advanced Processing Techniques for Fabrication of 3-D Microstructures for Future Electronic Devices," DARPA, N66001-01-C-8034, $125,000
9. Baker, R. J., (2004-2005) "Multi-Purpose Sensors for Detection and Analysis of Contaminants" EPA, X-97031102, $75,000
10. Baker, R. J., (2001-2006) Multi-University Research Initiative (MURI), "The effects of radio frequency pulses on electronic circuits and systems," Air Force Research Laboratory, $350,000.

Referred Conference Papers and Magazine Articles:

1. Montierth, D., Strand, T., Leatham, J., Linder, L., and Baker, R. J., "Performance and Characteristics of Silicon Avalanche Photodetectors in the C5 Process," submitted to the *55th Midwest Symposium on Circuits and Systems*, August 5-8, 2012.

2. VanAckern, G., Baker, R. J., Moll, A. J., and Saxena, V. "On-Chip 3D Inductors using Thru-Wafer Vias," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.

3. Yap, K. and Baker, R. J., "Two Techniques to Reduce Gain and Offset Errors in CMOS Image Sensors using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April 20, 2012.

4. Labaziewicz, A. and Baker, R. J., "A 2 GHz Effective Sampling Frequency K-Delta-1-Sigma Analog-to-Digital Converter," *Proceedings of the 54th Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**

5. Saxena, V., Balagopal, S., and Baker, R. J., "Systematic Design of Three-Stage Op-amps using Split Length Compensation," *Proceedings of the 54th Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**

6. Harvard, Q. and Baker, R. J., "A Scalable I/O Architecture for Wide I/O DRAM," *Proceedings of the 54th Midwest Symposium on Circuits and Systems*, August 7-10, 2011**.**

7. Wald, S., Baker, R. J., Mitkova, M., and Rafla, N., "A Non-Volatile Memory Array Based on Nano-Ionic Conductive Bridge Measurements," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 43-46, April 22, 2011.
8. Saxena, V. and Baker, R. J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband ADCs," proceedings *of the 53rd Midwest Symposium on Circuits and Systems*, August 1-4, 2010**.**
9. Saxena, V. and Baker, R. J., "Indirect Compensation Techniques for Three-Stage Fully-Differential Op-Amps ," (invited) proceedings *of the 53rd Midwest Symposium on Circuits and Systems*, August 1-4, 2010**.**
10. Harvard, Q., Baker, R. J., and Drost, R., "Main Memory with Proximity Communication: A Wide I/O DRAM Architecture," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 40-43, April 16, 2010.
11. Yap, K. M. and Baker, R. J., "Gain Error Correction for CMOS Image Sensor using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 52-55, April 16, 2010.
12. Gagliano, C. and Baker, R. J., "A Compact Delay-Locked Loop for Multi-Phase Non-Overlapping Clock Generation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, poster, April 16, 2010.
13. Montierth, D., Yap, K., and Baker, R.J., "CMOS Image Sensor using Delta-Sigma Modulation," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
14. Saxena, V. and Baker, R.J., "Synthesis of Higher-Order K-Delta-1-Sigma Modulators for Wideband Analog to Digital Conversion," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
15. Li, K., Saxena, V., Zheng, G., and Baker, R.J., "Full Feed-Forward K-Delta-1-Sigma Modulator," *4th Annual Austin Conference on Integrated Circuits & Systems*, Oct. 26-27, 2009.
16. Bollschweiler, L., English, A., Baker, R.J., Kuang, W., Chang, Z.-C., Shih, M.-H., Knowlton, W.B., Hughes, W.L., Lee, J., Yurke, B., Cockerham, N.S., and Tyree, V.C., "Chip-Scale Nanophotonic Chemical and Biological Sensors using CMOS Process," proceedings *of the 52nd Midwest Symposium on Circuits and Systems*, pp. 413-416, August 2-5, 2009**.**
17. Saxena, V., Li, K., Zheng, G., and Baker, R.J., "A K-Delta 1-Sigma Modulator for Wideband Analog to Digital Conversion," proceedings *of the 52nd Midwest Symposium on Circuits and Systems*, pp. 411-415, August 2-5, 2009**.**

18. Saxena, V. and Baker, R.J. "Indirect Compensation Techniques for Three-Stage CMOS Op-amps," proceedings *of the 52nd Midwest Symposium on Circuits and Systems*, pp. 9-12, August 2-5, 2009**.**
19. Regner, J., Balasubramanian, M., Cook, B., Li, Y., Kassayebetre, H., Sharma, A., Baker, R.J., Campbell, K.A., "Integration of IC Industry Feature Sizes with University Back-End-of-Line Post Processing: Example Using a Phase-Change Memory Test Chip," P*roceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 28-31, April 2009.
20. Gupta, S. Saxena, V., Campbell, K.A., and Baker, R.J., "W-2W Current Steering DAC for Programming Phase Change Memory," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 59-62, April 2009.
21. Rapole, H., Rajagiri, A., M. Balasubramanian, Campbell, K.A., and Baker, R.J., "Resistive Memory Sensing Using Delta-Sigma Modulation," *Proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 63-66, April 2009.
22. Kassayebetre, H., Regner, J., Rajagiri, A., Sharma, A., Hay, R.R., Baker, R.J., and Campbell, K.A., "Surface Acoustic Wave Device Fabrication using Zinc Oxide and Chalcogenide Thin Films**,"** poster presentation at the *IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, April, 2009.
23. Ande, H.K., Busa, P., Balasubramanian, M., Campbell, K.A., and Baker, R.J., (2008) A New Approach to the Design, Fabrication, and Testing of Chalcogenide-Based Multi-State Phase-Change Nonvolatile Memory, *proceedings of the* 51st *Midwest Symposium on Circuits and Systems*, pp. 570-573, August 10-13, 2008**.**
24. Saxena, V., and Baker, R.J., (2008) Compensation of CMOS Op-Amps using Split-Length Transistors, proceedings *of the* 51st *Midwest Symposium on Circuits and Systems*, pp. 109-112, August 10-13, 2008**.**
25. Saxena, V., and Baker, R.J., (2008) Indirect Compensation Technique for Low-Voltage Op-Amps, proceedings *of the* 3rd *Annual Austin Conference on Integrated Systems and Circuits (ACISC)*, May 7-9, 2008**.**
26. Cahoon, C., and Baker, R.J., (2008) Low-Voltage CMOS Temperature Sensor Design using Schottky Diode-Based References, *proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED)*, pp. 16-19, April 2008.
27. Saxena, V., and Baker, R. J., (2006) *Indirect Feedback Compensation of CMOS Op-Amps*, proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 3-4, April 2006.

28. Duvvada, K., Saxena, V., and Baker, R. J., (2006) *High Speed Digital Input Buffer Circuits*, proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 11-12, April 2006.
29. Saxena, V., Plum, T.J., Jessing, J.R., and Baker, R. J., (2006) *Design and Fabrication of a MEMS Capacitive Chemical Sensor System*, proceedings of the IEEE/EDS Workshop on Microelectronics and Electron Devices (WMED), pp. 17-18, April 2006.
30. Gorseth, T.L., Estrada, D., Kiepert, J., Ogas, M.L., Cheek, B.J., Price, P.M., Baker, R.J. Bersuker, G., Knowlton, W.B., *Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation*, presented at the Workshop on Microelectronic Devices (Boise, Idaho; April 14, 2006)
31. Gribb, M., Plumlee, D., Moll, A., Hill, H., Hong, F., Baker. J., Loo, S.M., Walters, R. and Imonigie, J., (2006) *An In-Situ Ion Mobility Spectrometer Sensor System for Detecting Gaseous VOCs in the Vadose Zone*, *Fourth International Conference on Unsaturated Soils* (*UNSAT '06*) *Conference, April 2-6, 2006, Carefree, AZ.*
32. Gribb, M., H. Hill. J. Baker, S.M. Loo, A. Moll, (2005), Ion Mobility Spectrometer (IMS) Sensor Project, presented at the Environmental & Subsurface Science Symposium, Inland Research Alliance, Sept. 19-21, 2005, Big Sky, Montana.
33. Ogas, M.L., Price, P.M., Kiepert J., Baker R.J., Bersuker G., and Knowlton W.B., (2005) *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, October 2005.
34. Butler, D.L, and R.J. Baker, (2005) *Low-Voltage Bandgap Reference Design Utilizing Schottky Diodes*, 2005 Midwest Symposium on Circuits and Systems.
35. Cheek, B.J., R.G. Southwick III, M.L. Ogas, P.E. Nagler, D. Whelchel, S. Kumar, R. J. Baker, W.B. Knowlton, (2004) *Preliminary Soft Breakdown (SBD) Effects In CMOS Building Block Circuits*, poster presentation at 2004 IEEE International Integrated Reliability Workshop, Oct. 18-21.
36. Ogas, M., R. Southwick, B. Cheek, C. Lawrence, S. Kumar, A. Haggag, R. J. Baker, and W. B. Knowlton, (2004) *Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra Thin Oxides*, poster presentation at Workshop on Microelectronics and Electron Devices, Boise, Idaho, April 16, 2004.
37. Ogas, M. L., R. G. Southwick III, B. J. Cheek, R. J. Baker, G. Bersuker, W. B. Knowlton, (2004) *Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices*, in proceedings of the 2004 IEEE International Integrated Reliability Workshop, pp. 32-36.

38. Cheek, Betsy J., Nate Stutzke, Kumor Santosh , R. Jacob Baker, Amy J. Moll and William B. Knowlton, (2004) Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics, 2004 IEEE International Reliability Physics Symposium, April, 25-29.
39. Stutzke, Nate, Betsy J. Cheek, Miles Wiscombe, Terry Lowman, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, (2003) *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, 2003 IEEE International Integrated Reliability Workshop, Oct, 20-23.
40. Ogas, M. L., R. G. Southwick, B. J. Cheek, C. E. Lawrence, S. Kumar, A. Haggag, R. J. Baker, W. B. Knowlton (2003) *Investigation of Multiple Waveform Pulse Voltage Stress (MWPVS) Technique in Ultra-Thin Oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop Oct, 20-23.
41. Baker, R.J., (2003) *Mixed-Signal Design in the Microelectronics Curriculum*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
42. J.A. Hartman, R.J. Baker, M. Gribb, H.H. Hill, J. Jessing, A. Moll, W. Prouty, D. Russell, (2003) *A Miniaturized Ion Mobility Spectrometer (IMS) Sensor for Wireless Operation*, FAME (Frontiers in Assessment Methods for the Environment) Symposium, Sponsored by NSF, Minneapolis, Minnesota, August 10-13, 2003.
43. Lawrence, C.E., B.J. Cheek, T.E. Lawrence, Santosh Kumar, A. Haggag, R.J. Baker, and W.B. Knowlton, (2003) *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2.
44. Betsy Cheek, Carrie Lawrence, Tim Lawrence, Jose Gomez, Theodora Caldwell, Dorian Kiri, Santosh Kumar, Jake Baker, Amy J. Moll, and William B. Knowlton, (2002) *Gate Dielectric Degradation Effects on nMOS Devices and Simple IC Building Blocks (SICBBs)*, IEEE Electron Devices Society Boise Meeting, Boise, ID Oct. 25.
45. Lawrence, C., B. Cheek, T. Caldwell, T. Lawrence, D. Kiri, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, (2002) *Pulse voltage stressing of ultrathin gate oxides in NMOS devices, poster session at IEEE International Integrated Reliability Workshop,* October 21-24.
46. Cheek, B., C. Lawrence, T. Lawrence, T. Caldwell, D. Kiri, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, (2002) Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter, poster session at IEEE International Integrated Reliability Workshop, October 21-24.

47. Baker, R.J., (2002) "Sensing Circuits for Resistive Memory," *IEEE Electron Devices Society* Meeting, Boise, Idaho October 25, 2002.
48. Rivera B., Baker R. J., Melngailis J., (2001) "Design and Layout of Schottky Diodes in a Standard CMOS Process," 2001 International Semiconductor Device Research Symposium, Washington DC, Dec. 2001.
49. Hess, H. and R. Baker, (2000) "Easier Method to Simultaneously Trigger Series-Connected MOS Devices," *Power Systems World Conference* 2000, Boston, Massachusetts, September 2000.
50. Baker, R.J., and H. Hess, (1999) "Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices." *International Electric Machines and Drives Conference,* Seattle, Washington, May 1999, pp. 673-676.
51. Baker, R.J., (1999) "A windows based integrated circuit design tool for distance education," *International Conference on Simulation and Multimedia in Engineering Education*."
52. Chen H. and Baker R.J., (1998) "A CMOS Standard-Cell Library for the PC-based LASI Layout System," *1998 Midwest Symposium on Circuits and Systems.*
53. Liu, S., and Baker, R.J., (1998) "Process and temperature performance of a CMOS beta-multiplier voltage reference," *Proceedings of the 41st Midwest Symposium on Circuits and Systems," August 9-12, 1998.*
54. Boyce D.E. and Baker R.J., (1997) "A Complete Layout System for the PC," *1997 Midwest Symposium on Circuits and Systems.*
55. Baker, R.J., and Blair, J.J., (1991) "Step response considerations and the design of a suitable step generator for high speed digitizer testing," *LLNL's Third Annual Workshop on High Speed Digitizers*, April 3-4, Las Vegas, Nevada.
56. Baker, R.J., (1990) "Step-recovery diodes sharpen pulses," *Engineering Design News Magazine*, pp. 154-156, May 10.

Professional Associations and Achievements

- Member, ASEE
- Member, IEEE (student, 1983; member, 1988; senior member, 1997, Fellow, 2013), Societies: Circuits and Systems, Education, Instrumentation and Measurement, Solid State Circuits
- Member of the Electrical Engineering honor society Eta Kappa Nu
- Licensed Professional Engineer

Honors and Awards

- Distinguished Lecturer for the IEEE Solid-State Circuits Society, 2013-present
- Tau Beta Pi UNLV Outstanding Professor of the Year, 2013
- IEEE Fellow for contributions to the design of memory circuits - 2013
- IEEE Circuits and Systems (CAS) Education Award-2011
- Elected to the Administrative Committee of the Solid-State Circuits Society, 2011-present
- Frederick Emmons Terman Award from the American Society of Engineering Education – 2007.
- President's Research and Scholarship Award, Boise State University – 2005.
- Honored Faculty Member – Boise State University Top Ten Scholar/Alumni Association 2003.
- Outstanding Department of Electrical Engineering Faculty, Boise State 2001.
- Recipient of the IEEE Power Electronics Society's Best Paper Award in 2000.
- University of Idaho, Department of Electrical Engineering outstanding researcher award, 1998-99.
- Elevated to Senior member of the IEEE, 1997
- University of Idaho, College of Engineering Outstanding Young Faculty Award, 1996-97.

Service

- Reviewer for IEEE transactions on solid-state circuits, circuits and devices magazine, education, instrumentation, nanotechnology, VLSI, etc. Reviewer for several American Institute of Physics journals as well (Review of Scientific Instruments, Applied Physics letters, etc.) Board member of the IEEE press (reviewed dozens of books and book proposals). Solid-State Circuits Society Administrative Committee. Reviewer for the National Institutes of Health. Technology editor for the Solid-State Circuits Magazine.
- Led the Department on ABET visits, curriculum and policy development, and new program development including the PhD in electrical and computer engineering. Provided significant University and College service in infrastructure development, Dean searches, VP searches, and growth of academic programs. Provided university/industry interactions including starting the ECE department's advisory board. Held positions as the ECE department Masters graduate coordinator and coordinator for the Sophomore Outcomes Assessment Test (SOAT).

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